ABSTRACT OF THE DISCLOSURE

A semiconductor memory device including a flash memory and a RAM incorporating a pseudo-SRAM contained in an MCP, has an internal transfer control signal for controlling internal data transfer between the flash memory and pseudo-SRAM, and an external transfer control signal for controlling data transfer between an external CPU and pseudo-SRAM, as control signals for the pseudo-SRAM. A flash controller in the RAM controls the internal transfer control signal so as to suspend the internal data transfer between the flash memory and pseudo-SRAM when the external CPU requests access to the pseudo-SRAM during the internal data transfer.